LOW POWER VITERBI DECODER DESIGN BASED ON REVERSIBLE LOGIC GATES

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Abstract—
InrecenttrendsofVLSItechnologythereversible logic has became the major area of research in optimization of area,powerandspeedconstraints.Thereversiblelogichasequal number of inputs and outputs. In wireless communications Viterbi algorithm is employed to have minimal number of communication channels. The Viterbi decoder design at 65nm technology using reversible logic has made an attempt for optimizing power, areaanddelaywithincreasedefficiency.

Keywords— Viterbi decoder, Reversible logic, Feynman Gate, Peres Gate, HN Gate, Power consumption, Delay.

I. INTRODUCTION

The Viterbi decoding algorithm was proposed by Andrew J Viterbi, which is a decoding process for convolutional codes in memory-less noise. This algorithm is implemented in the designing of communication systems. The Viterbi Algorithm is the most resource consuming and it finds the most-likely noiseless state transition sequence in a state diagram, given a sequence of symbols which are interrupted by noise[1].

Generally, a viterbi decoder consists of three basic computation units: Branch Metric Unit (BMU), Add- Compare-Select Unit (ACSU) and Survivor Memory Unit (SMU) [2].

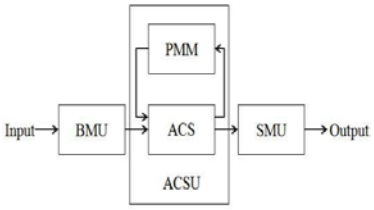


Figure 1. Block diagram of Viterbi decoder

The primary unit is called as Branch Metric Unit (BMU). This unit will compare the received data symbols with the ideal outputs of the encoder and finally the branch metric will be calculated. The Euclidean distance or Hamming distance is utilized for the calculation of branch metric. The BMU creates branch metrics for the following module in terms of the symbols which are received by thechannel.

The Add Compare Select Unit (ACSU) is illustrated as the sum of the Branch Metrics (BM) to the subsequent Path Metrics (PM). The new PM will be compared and the selected PM will be stored in the Path Metric Memory (PMM). At the same time, the ACSU stores the associated survivor path decisions in the Survivor Memory Unit (SMU).The PM of the survivor path of each state is updated and stored back into the PMM.

The Survivor Memory Unit uses the Trace-Back method to identify the survivor path

and output data. In this unit the decoded bits are extracted from the beginning through
Minimum path metric. At the beginning state, backward tracing is followed by the survivor path, which initially contributed to the current PM and a unique path is identified. While tracing back through the trellis, the decoded output sequence corresponding to the traced branches is generated in the reverseorder.

II. REVERSIBLE LOGIC

Reversible computing is the application of principles of recycling to computing. A reversible logic gate is mapped with one-to-one logic device having an n-input, n-output gate. As it helps to find out the outputs from inputs although the inputs can be exclusively recovered from the outputs. In the necessary conditions to have the number of inputs equal to the number of outputs additional inputs or outputs is added. An important constraint present on the design of a reversible logic circuit using reversible logic gate is that the fan-out is not allowed. The quantum cost of reversible logic circuits must be minimum. With the minimum number of reversible gates the design of reversible circuit is accomplished. The major constraint to attain optimization of the circuit is to produce the garbage outputs and the constant inputs with the minimum number.

The reversible logic gates are the circuits which has number of inputs is equal to number of outputs. The important optimization parameter for every reversible logic gate is the quantum cost[3].

The important reversible logic gates which are required for designing Viterbi decoder are.

A. FeynmanGate

The Feynman gate is 2x2 reversible gate which has the inputs (A, B) and the outputs (P =A, Q = A B). This gate is also referred as Controlled NOT. The quantum cost is 1. This is mainly used for the fan-out function. The power consumption and delay are 18mW and 7.760ns[4].

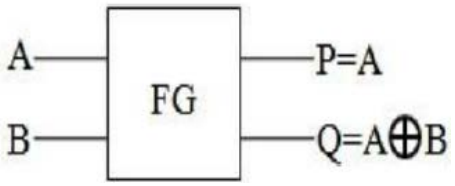
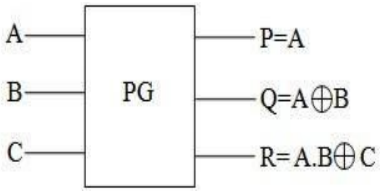


Figure 2. Feynman Gate

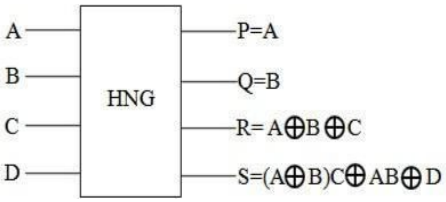
B. PeresGate

The Peres gate is 3x3 reversible gate, where the inputs are A, B, C and the outputs are P, Q and R. The outputs are mapped as P =A, Q = A B and R= A.B C. The quantum cost is 4. The power consumption and delay are 24mW and 7.824ns.

A. HN Gate



The HNG is a 4x4 reversible gate, and abbreviated as Haghparast Navi Gate (HNG). It has 4 inputs A, B, C, D and 4 outputs P, Q, R, S, its mapping is P=A, Q= B, R= A B C and S= (A B) C AB D. The quantum cost is 6. The power consumption and delay are 24mW and7.824ns.



III. PROPOSED VITERBI DECODERUSING REVERSIBLE LOGICGATES

In proposed system the calculation of metric, addition, comparison of weight and selection of survivor path everything is carried out in the ACS array (ACSU). Thus the ACS array contains the values of weight at every state, as a progression along the survivor path. The codewords are very much required when comparing with different codewords of different paths, to identify the survivor path. The functions of compilation and comparison takes place within the ACS array which actually identifies the extensions of path. The signals

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determining these extensions to the survivor paths are passed from the ACS array to the SPU, which then updates the survivor paths.

The Figure 5 shows the top level RTL design of Viterbi decoder in which U1 indicates compute metric unit, U2 represents metric unit, U3- acs enable unit, U4- compare select unit, U5- reduce unit and U6- path memory unit

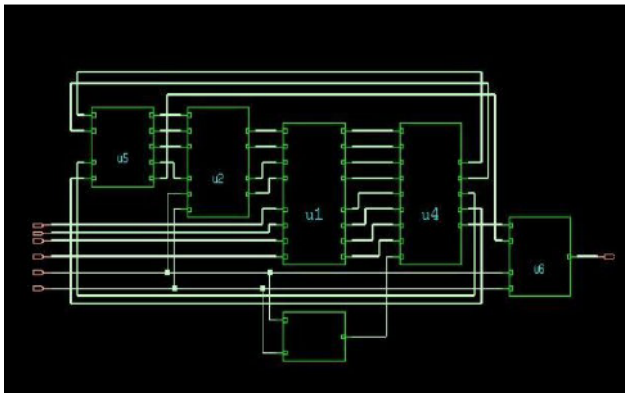

Figure 5. Top Level RTL design of Viterbi Decoder using Reversible Logic Gates

The design has the four input signals each signal having two bits with clock and reset signals. As the Reversible Logic gates reduces the power consumption and path delay, the PG will function as half adder and HNG will function as full adder.

A. Compute Metric Unit

In the compute metric unit, each received code word and each excepted code word (metric output) will be the inputs for this unit in which if performs the comparison between the code words and generates a codeword which is the input for the compare selectunit.

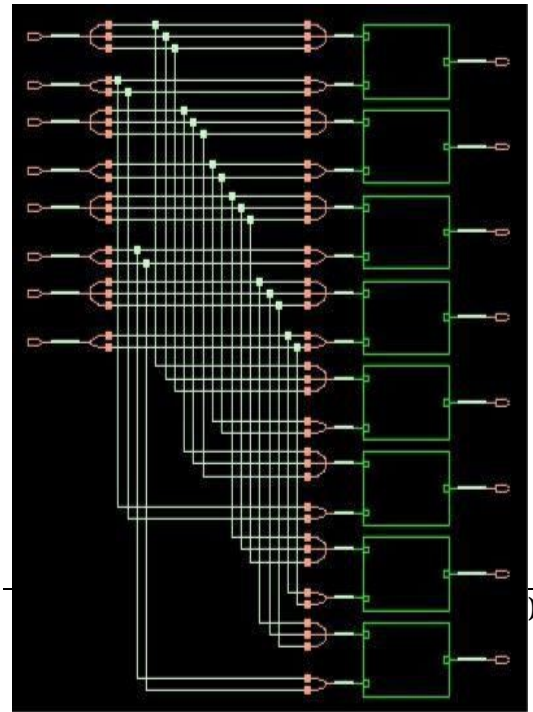

Figure 6. RTL design of Compute Metric Unit

The Figure.7 shows a unit of compute metric in which expected bits are represented as a [0:2] and received bits as

b [0:1]. The blocks U_FA_0 and U_FA_2 is implemented by Peres gate which performs the half adder and U_FA_1 is implemented by HNG performing full adder.

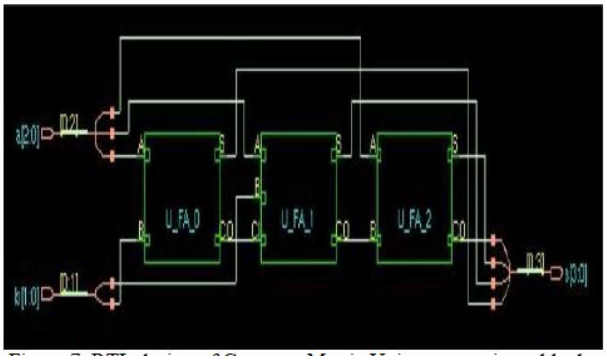

Figure 7. RTL design of Compute Metric Unit representing a block

Each bit of the metric unit will be the inputs for the 3 sub units and user input of 2 bits will be for the inputs for U_FA_0 and U_ FA_ 1. The U_FA_0 will generates the output of 2 bits, one bit will be the final output of the block and other bit will be the input for the next sub unit i.e. U_FA_1. The U_ FA_1 will generates the output of 2 bits, one bit will be the final output of the block and other bit will be the input for the next sub unit i.e. U_FA_2. Similar function is performed by the U_FA_2 sub unit and both the outputs. The unit has 8 blocks and each block performs the same function as explained above. Hence the compute metric has 8 outputs with each output of 4 bits.

B. Metric Unit

The metric unit performs the storage operation of the expected code word. The Figure 8 shows the RTL design in which it has the cock and reset signals for each metric unit

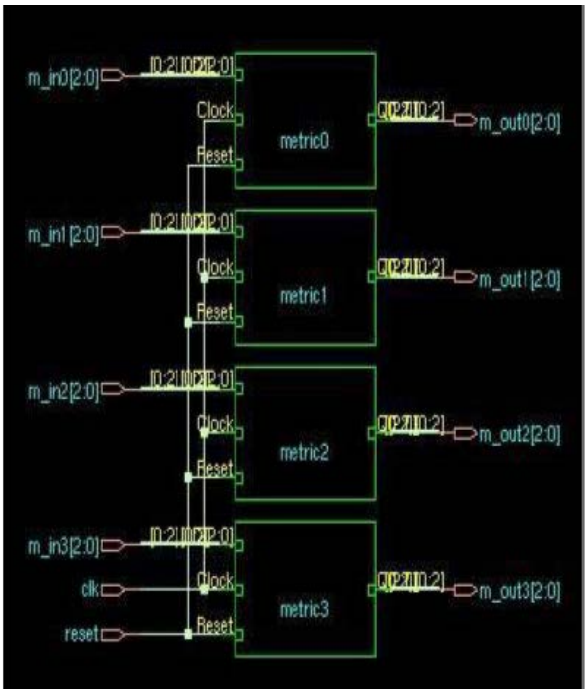

Figure 8. RTL design of Metric Unit

The metric unit stores the minimum metric of the oldest bits as it is required for next computation cycle. Every time the oldest path will be erased and the new minimum reduced metric will be updated. The unit has 4 metric blocks and each metric block has 3 inputs and3outputs.

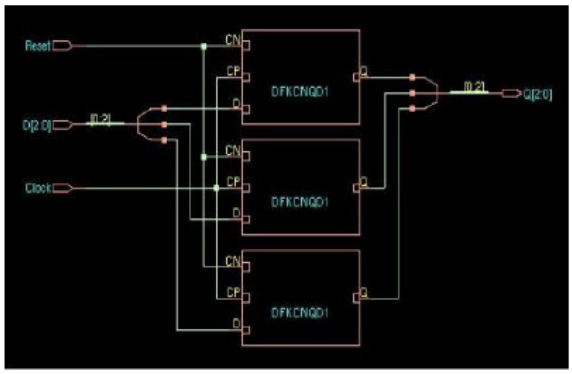

Figure 9 represents the each metric unit which consists of three D flip-flops, once the clock signal is applied upon reset=1 the bits will perform the comparison operation in the compute metricunit.

C. ACS EnableUnit

Figure 10 shows the acs-enable unit which consists of D flip-flops which has clock and reset signals and initially the reset will be 0, D input is0.

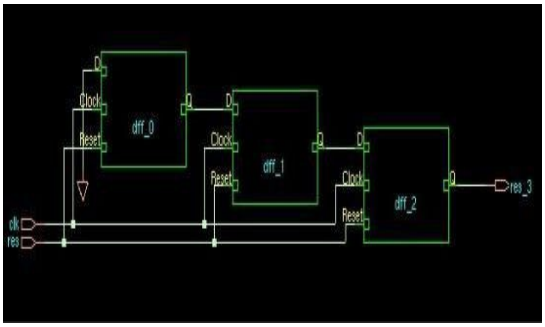

Figure10.RTLdesignofACS-EnableUnit

Once the reset value becomes 1 the unit will send a signal such that a compare-select unit isenabled.

D. Compare SelectUnit

The codeword which is received from the compute metric unit will have maximum path metric such that the minimum path metric has to be calculated by selecting the appropriate metric, this operation in performed by the compare select unit and Figure 11 shows the RTL design of theunit.

Upon receiving the acs enable signal this unit will be enabled and the each received codeword from the compute metric unit will be of 4 bits. Two code words will be added and compared such that minimum metric will be calculated and obtained by performing the logical operations such as AND and OR. Finally the minimum metric will be selected and the codeword will be three bits. The output will be of four bits which will be stored in the path memory. The minimum metric which is calculated will be reduced such that previous path will be deleted. The path metric of both inputs will be compared and the metric with smallest distance will be the output and this is considered as the control signal for the path memoryunit.

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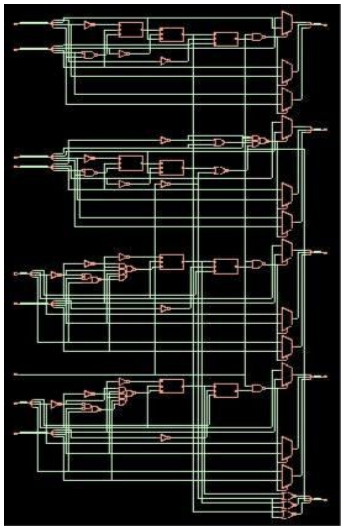

Figure 11. RTL design of Compare Select Unit

E. Reduce Unit

The minimum path metric which is obtained has to compared with the oldest path metric and it will be stored in the reduce unit, suppose if both the metric are equal then the oldest path metric will be retained otherwise the new minimum path metric will be stored in the reduceunit

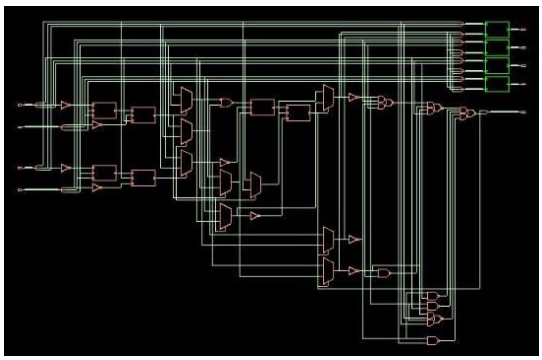

Figure 12. RTL design of Reduce Unit

The old minimum path metric which is stored will be evaluated with the HN and Feynman reversible gates such that the new minimum metric of 3 bits will be stored by eliminating the oldestpath.

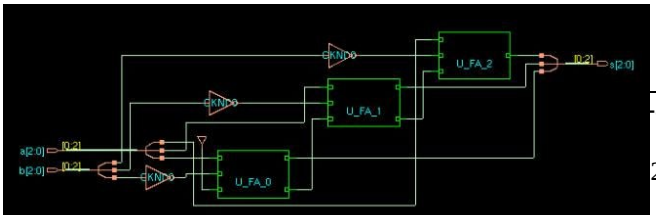

Figure 13. RTL design of Reduce Unit for two inputs(0 down to 2)

The control signal of 2 bits is required for the path memory to enable the unit and this is generated by the reduce unit by latch which consists of OR and AND logicalgates

F.Path MemoryUnit

The path memory unit consists of 4x1 multiplexer units and the D flip -flops. The control signal is considered as a select signal for the multiplexer as it is used to select the minimum path metric of the decoded message bit.

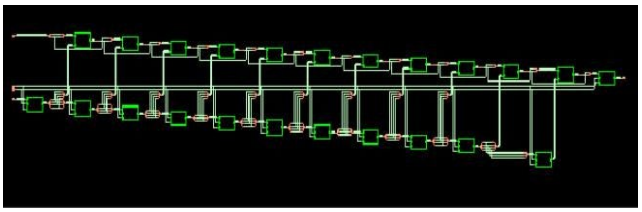

Figure 14. RTL design of path memory unit

The input for the D- flip flop is the ACS signal which is the output from the compare-select unit of 4 bits. These bits are considered as a survival bit inputs for the 4x1 multiplexer.

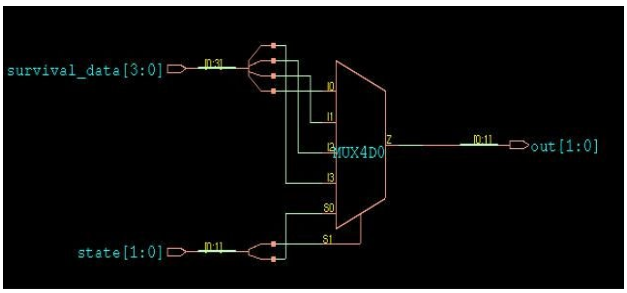

Figure 15. 4x1 Multiplexer unit

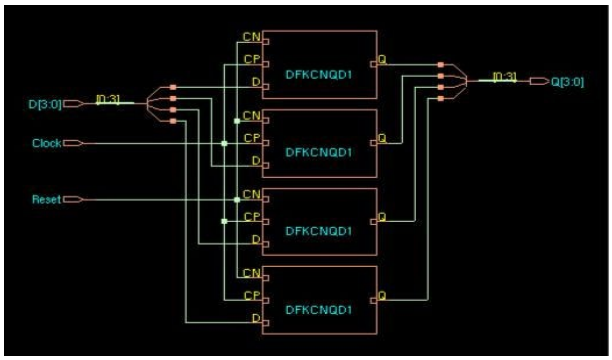

Figure 16. Buffer unit with D-flip flop

During the initial stage the path 1 is identified, then path 2 is identified by the multiplexer units. The unit consists of 11 multiplexer units and 9 D flip-flops.

The decoder output will be available at the receiver end after the completion of 14 clock cycles. Since the clock and reset signal are applied to the acs enable and path memory units.

IV. RESULTS AND DISCUSSION

The proposed Viterbi decoder is developed by Verilog coding and simulated. The main constraints for VLSI design is area, speed and power. The power performance report is shown in Table 1, area and timing performance report is tabulated in Table2.

INSTANCE	Power Analysis in ηW		
	Leakage Power	Dynamic Power	Total Power
U1 [Compute Metric]	1436.774	4871.918	6308.693
U2[Metric]	555.193	2961.352	3516.545
U3[ACS_Enable]	157.896	298.383	456.279
U4[Compute Select]	520.295	3986.532	4506.828
U5[Reduce]	1000.059	5939.455	6939.514
U6[Path Memory]	2697.978	11326.026	14024.004
VITERBI [TOP LEVEL]	**6368.196**	**30094.526**	**36462.722**

Table 2. Area and Timing Performance Summary

INSTANCE	Number of Cells	Area (sq microns)	Time Delay (psec)
U1 [Compute Metric]	40	173	320
U2[Metric]	12	86	135

The functionality of Viterbi decoder using reversible logic gates is verified and simulated. The simulation waveform result is shown in Figure17.

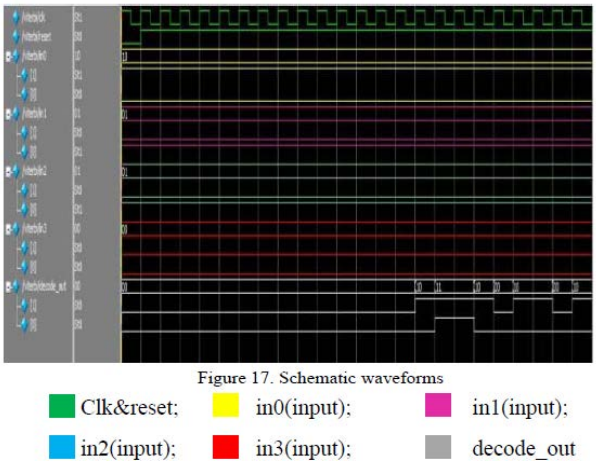

Figure 17. Schematic waveforms

V. CONCLUSION

The Viterbi decoder which consists BM, ACS and SM Units have been implemented by considering the reversible logic gates such as Feynman, Peres and HN gates to achieve a better efficiency. The designing is done using HDL coding and synthesized in CADENCE tool. The performance summary such as area, power efficiency and delay results are achieved. Hence this design can be used in high speed communicationapplications.

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